EFFECTS OF TOTAL DOSE IONIZING RADIATION ON THE 1802 MICROPROCESSOR*

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Summary

Several versions of the 1802 CMOS microprocessor were subjected to Co-60 irradiations. Total dose data is provided for production line parts from two vendors, a specially processed radiation hard lot, and one developmental SOS unit. The increase in total dose failure level from 1×10^4 to 5×10^5 rads(Si) for the specially processed parts proves the feasibility of hardening the Si-gate LSI technology used for the 1802.

Introduction

The 1802 microprocessor, which is functionally illustrated in Figure 1, is of interest for many military and space system requirements. This is primarily because of the several inherent advantages of the CMOS technology over other LSI technologies; that is, low power consumption, high noise immunity and wide temperature tolerance. For example, the 1802 device is one of the few MOS microprocessors now specified for operation over the full military temperature range of -55 to 125° C. However, the 1802 also has several other important features; it requires only a single voltage supply, operates with a single phase clock and is completely static. Additional advantages are that there are second sources for the part, a silicon-on-sapphire (SOS) high speed 1802 is to be commercially marketed, and implementation of previously developed radiation hardening processing techniques is possible.

Previous testing at NRL[1] of the 1801 microprocessor, the early two chip version of the 1802, indicated that catastrophic failure occurred at radiation levels between 1×10^4 and 3×10^4 rads(Si) for a 5 volt supply and typical devices. One 1801 set which had a very high initial leakage current, but which operated functionally, failed between 1×10^3 and 2×10^3 rads(Si). The failure levels for the current 1802 product are found to be consistent with the previous 1801 results: that is, for typical devices functional failure occurs at about 1×10^4 rads(Si) for a 5 volt irradiation bias. For a 10 volt irradiation bias the functional failure level is about 7×10^3 rads(Si). Again, an atypical unit was found to fail at a lower dose.

TABLE I

Summary of 1802 tests.

VENDOR	PROCESSING	PACKAGE CODE	# TESTED	IRRAD. BIAS (VOLTS)	IRRAD. COND.*	FAILURE LEVEL (RADS(Si))
1	SOS	7604AF	1	5	E	1.2×10^4
1	PROD.	7622	3	10	C+UC	$\sim 7.0 \times 10^3$
1	PROD.	K640	1	5	E	1.5×10^4
1	PROD.	645	3	10	C+UC	$\sim 7.0 \times 10^3$
1	PROD.	649	2	5	C	$\sim 9.0 \times 10^3$
1	PROD.	649	2	5	E	9.0×10^3
1	PROD.	7653	2	5	E	9.5×10^3
2	PROD.	EARLY 77	2	5	E	8.0×10^3
1	SPECIAL	7702K	2	5	C	$2\text{-}5 \times 10^5$
1	SPECIAL	7702K	2	5	E	5.0×10^5

* C = Clocked and asynchronously reset.
UC = Clock input high and pulsed reset.
E = Registers initialized and microprocessor exercised.

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Experiment

There were four types of 1802s tested in this experiment. A summary of the devices tested as well as the failure level for each package code is provided in Table I.

The production line parts from vendor #1 were all obtained by off-the-shelf purchases. No special screening, testing or burn-in was imposed. Some of the parts in the early lots exhibited anomalously high leakage current or propagation delays which were either significantly longer or shorter than the average. Some of these parts did not operate properly in 1802 systems. Such devices were not included in the radiation tests with the exception of one device from lot 7622 which was found to fail some of the functional tests at about the 3×10^3 rad(Si) level rather than the 7×10^3 rad (Si) level given in Table I. It is suggested that in order to meet the failure levels given in Table I, an electrical screen should be implemented to eliminate any atypical devices.

The 1802s from vendor #2 were obtained from early production runs and may not be entirely representative of the final production parts. Although vendor #2's process is not quite the same as vendor #1's process, there are no differences which would be expected to significantly impact radiation hardness.

The SOS part included in this experiment is an early developmental model fabricated using a standard, non-hardened process. The fact that it was more radiation tolerant than the bulk production units is quite encouraging.

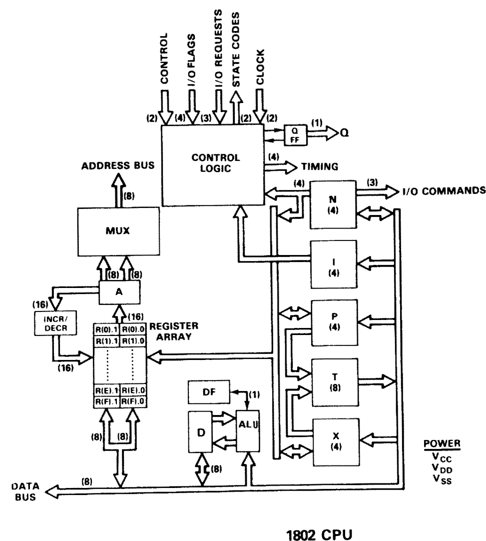

Figure 1. Functional block diagram of the 1802 microprocessor.

A specially processed lot of 1802s was included in this experiment. Figure 2 indicates the changes made to the standard production process for the purpose of increasing total dose hardness. Primarily, high temperature processing steps were replaced by lower temperature processing steps. And, in addition, electron beam aluminum evaporation was replaced by evaporation from an induction heated boron-nitride crucible. Since the low temperature diffusion produced shallow junctions, silicon doped (1%) aluminum was used for the metallization to eliminate spiking.

- LOW-TEMPERATURE OXIDE
  - 850°C HCL - STEAM
  - 850°C N_2 ANNEAL
  - 700Å THICKNESS
- ION-IMPLANTATION FOR P^+ REGIONS
  - 850°C ACTIVATION-ANNEAL
- LOW-TEMPERATURE DIFFUSION
  - 950°C $POCL_3$ FOR N^+ REGIONS
- NON E-GUN METALLIZATION
  - IN-SOURCE EVAPORATION
  - SILICON-DOPED (1%) ALUMINUM

Figure 2. Process modifications used to fabricate radiation hardened 1802 microprocessors.

The testing was performed at several locations and under various irradiation bias conditions. The clocked and unclocked (C+UC) situation specified in Table I corresponds to the bias configuration shown in Figure 3. The clocked parts received a 1 MHz square wave clock signal and all parts were asynchronously cleared at 400 µS intervals. The devices which were exercised (E) during the irradiations were biased as shown in Figure 4. In this case, buffers were used to isolate the 1802s under test from the master 1802 as well as the other 1802s being irradiated. As indicated, each 1802 under test had its data bus driven by tri-state buffers which were turned on by the memory read pulse, $\overline{MRD}$, of the device under test. Clock frequency in this case was approximately 100 kHz. The actual program used to exercise the 1802s during irradiation is provided in Figure 5. This exercise program, besides initializing the 1802's internal registers, flashed a light-emitting -diode (LED) via the Q output so that at least a partial indication of whether or not a given 1802 was operating could be made during the irradiation. When an LED ceased flashing during the irradiation, the time was recorded so that a more exact failure level for the part could be determined. It was found that parts from the same lot failed this test at essentially identical times.

Over the course of the experiment several different types of test equipment were used. However, in all cases, a bench top set-up which included the RCA Microkit was utilized. This "tester" was used in two ways. First, it provided a quick indication of whether there were operating problems with the microprocessor in a simple system. Second, various time delay measurements were made on the 1802. If the microprocessor was able to operate the Microkit utility routine, a program was inserted into the Microkit from a teletype. This program contained a short loop which cleared one of the internal registers in the 1802, wrote a word into that register, then looped back. The waveforms at various pins of the 1802 were observed using an oscilloscope and some external circuitry which allowed triggering on a specific clock pulse after a fixed, presettable binary address appeared on the address lines. Figure 6 indicates the six time delays which were chosen to be measured in this way.

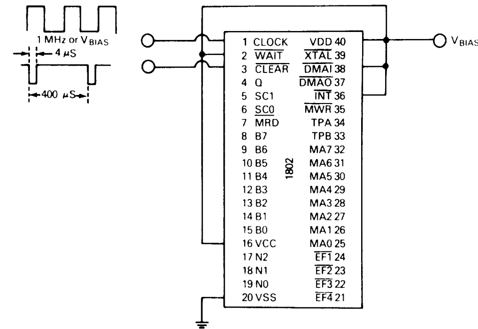

Figure 3. Clocked and unclocked 1802 irradiation bias conditions.

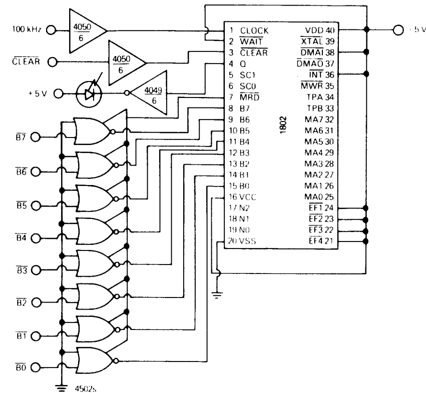

Figure 4. Irradiation bias configuration for exercised 1802s.

LINE	INSTRUCTION	LABEL	OPERATION	COMMENT
8000	C4	START	NOP	
8001	F8		LDI	SET PC TO 80XX
8002	80		80	
8003	B0		PHI	
8004	F8		LDI	LOAD ALL 1s IN R1-R7
8005	FF		FF	
8006	A1		PLO	
8007	B1		PHI	
.	.		.	
8012	A7		PLO	
8013	B7		PHI	
8014	F8		LDI	LOAD ALL 0s IN R8-RF
8015	00		00	
8016	A8		PLO	
8017	B8		PHI	
.	.		.	
8024	AF		PLO	
8025	BF		PHI	
8026	7B	EXERCISE	REQ	TURN LED OFF
8027	F8		LDI	
8028	0F		0F	
8029	B1		PHI	
802A	21	LOOP1	DEC	
802B	91		GHI	
802C	3A		BNZ	BRANCH TO LOOP1
802D	2A		2A	IF NOT ZERO
802E	7A		SEQ	TURN LED ON
802F	F8		LDI	
8030	0F		0F	
8031	B1		PHI	
8032	21	LOOP2	DEC	
8033	91		GHI	
8034	3A		BNZ	BRANCH TO LOOP2
8035	32		32	IF NOT ZERO
8036	30		BR	BRANCH TO EXERCISE
8037	26		26	

Figure 5. Irradiation exercise program for the 1802.

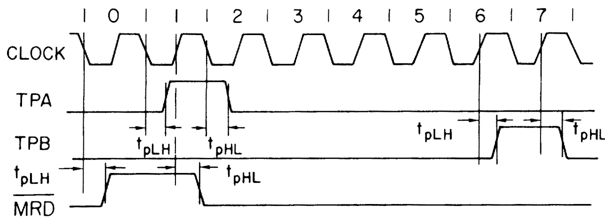

Figure 6. Definition of propagation delays measured on the 1802.

More comprehensive test information was obtained from two automated integrated circuit test systems, the Macrodata MD154 and the Teradyne J-283. The test programs used on the MD154 were the characterization programs developed at Macrodata[2] for the 1802. A shortened version of "RCA Characterization Tape, Final A" was used in some cases and an RCA modified version of the Macrodata test program was used at other times. In any case, the Macrodata test was primarily a functional test in which timing information was generated. This timing data could be correlated with the time delay measurements made using the Microkit by taking into account the differences in loading on the output pins.

The Macrodata program which was used consisted of several functional tests with provision for printout of the power supply voltage shmooed against the propagation delay to various outputs. For example, Figure 7 shows the shmoo plot of supply voltage versus propagation delay to the address lines, MA0 through MA7, utilizing functional pattern 2 after a 3×10^3 rads(Si) irradiation. Pattern 2 included all of the instructions which increment or decrement any register (except for 1N and 2N) and all of the branch and skip instructions. The dotted line indicates the additional pass area for this device pre-irradiation. The shmoo plot obtained after the 1×10^4 rad(Si) dose point had no observable pass area. The various functional tests performed on the MD154 provided little insight into how the microprocessors failed since essentially all tests indicated complete failure at the same dose points. For this reason, only some of the propagation delay data are included in this report.

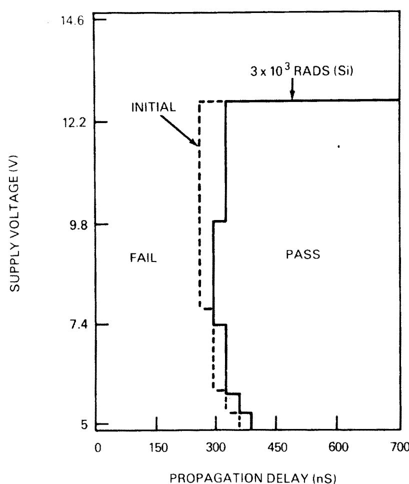

Figure 7. Shmoo plot of supply voltage versus propagation delay for address lines and functional pattern 2.

The most useful data came from the Teradyne test system. In this case, the test program provided a great deal of dc parametric information on the 1802 as well as checking for functional operation with supply voltages of 2.8, 3.5, 5, 7 and 15 volts. In addition, noise margin was checked using the functional test pattern at both 5 and 10 volts. Most of the data provided in this paper were obtained from this test system. In addition, the functional test information helped to pinpoint the functional failure levels given in Table I as well as the mechanism responsible for these failures.

Results

Threshold voltages were measured for the n- and p-channel transistors making up the oscillator inverter gate of the 1802. Figure 8 illustrates how the threshold voltages were affected by the irradiations for the various categories of samples included in this experiment. Since the oscillator gate was clocked with a square wave during the irradiations, the threshold data is not directly applicable for other transistors in the 1802 which were statically biased or which saw waveforms differing from square waves during irradiation. Nevertheless, the data clearly illustrates why there were differences found between the various types of 1802s in terms of functional failure level and failure mechanism.

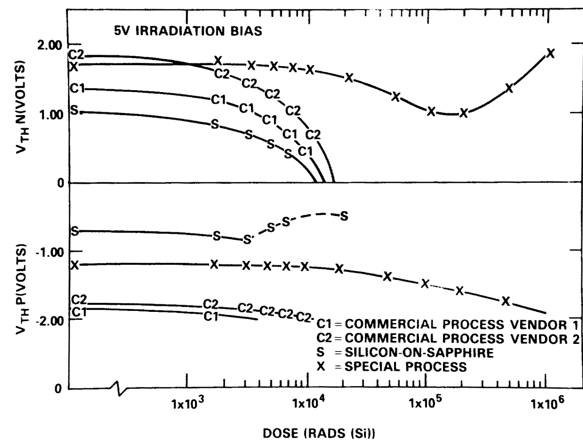

Figure 8. Threshold voltage versus total dose for 1802 devices.

There were five lots of production line devices included in this experiment from vendor #1; therefore, the C1 data points shown in Figure 8 are intended to be typical (the mean average) for vendor #1's product. For example, one lot of devices from vendor #1, K640, had an initial n-channel threshold of 2.3 volts (compared to the typical 1.4 volts) and, although, the threshold shifts for the K640 parts tracked the C1 curve, the dose point for the n-channel becoming depletion mode is somewhat greater than the value shown for C1 in the figure. This is reflected in the failure level for the K640 devices given in Table I, which is somewhat greater than the failure levels given for the other production units from vendor #1.

The threshold voltage curve for the special process n-channel transistor is typical of previous results for n-channel devices fabricated using radiation hardening processes.[3] That is, there is an initial decrease in threshold voltage as positive charge builds up in the gate oxide. This negative threshold shift is eventually overcome by the effect of interface state build-up which becomes important at about 10^5 rads(Si) and causes the n-channel threshold to increase. Thus, the n-channel transistor never becomes depletion mode.

The gross chip leakage current also was measured and this data is presented in Figure 9. Notice that there is a direct relationship between the n-channel threshold voltages passing through zero volts and the leakage current increasing dramatically. For the SOS device there is a rather large initial leakage current and the knee is not nearly as sharp as it is for the C1 and C2 curves. Such an initial leakage current is common for SOS devices because of edge and back surface problems. The rounded knee is probably caused by the fact that there is more variation in transistor characteristics on an SOS chip than there is on a bulk chip and, thus, a greater variation in the point where the n-channel transistors go into depletion.

The leakage current curve for the hardened devices is much differently shaped than the other leakage current curves, exhibiting a much slower increase in current and an eventual saturation at a fairly small level. The very steep slope observed for the other devices is not seen in this case because leakage current for these parts is not related to the n-channel thresholds passing through zero. This type of leakage current has been observed before and is caused by an increase in the reverse bias leakage current through the drain-channel junction of the p-channel transistors. Positive charge build-up in the oxide above this junction causes the n^+ channel edge to spread along the surface. The increase in interface states caused by radiation, which become significant at doses above 1×10^5 rads(Si), produces an increase in surface generation which is observed as an increase in reverse leakage current. The saturation leakage current for the chip is about 140 μA which turns out to be about 47 nA for each p-channel transistor on the 1802. This is a reasonable current for such an effect.

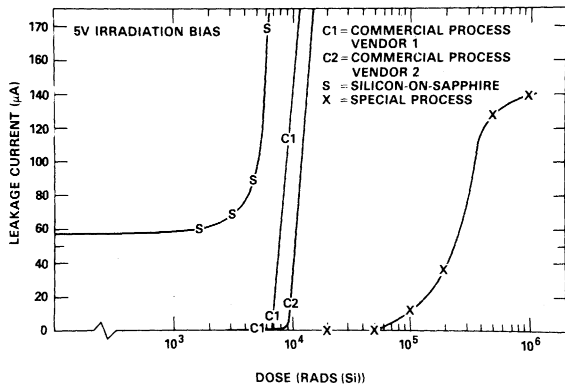

Figure 9. Total chip leakage current versus total dose for 1802 devices.

The output drive capability for n- and p-channel transistors versus total dose is shown in Figure 10. Notice that there are two differently sized p-channel devices on the outputs. There is very little change in the drive current for most of the parts. The radiation-hardened devices show a decrease in drive as the dose increases. This would seem to be due to the fact that the threshold voltage increases for the n-channels and decreases for the p-channels as the dose increases so that the gates do not turn on as hard: however, in addition, there may be a decrease in transistor transconductance due to interface state build-up which plays a part.

The propagation delay of the TPA transition from high to low, t_{pHL}, versus total dose is shown in Figure 11. Propagation delay decreases for the production and SOS devices and increases for the radiation-hardened devices reflective of the opposite variations in n-channel threshold voltage shown in Figure 8.

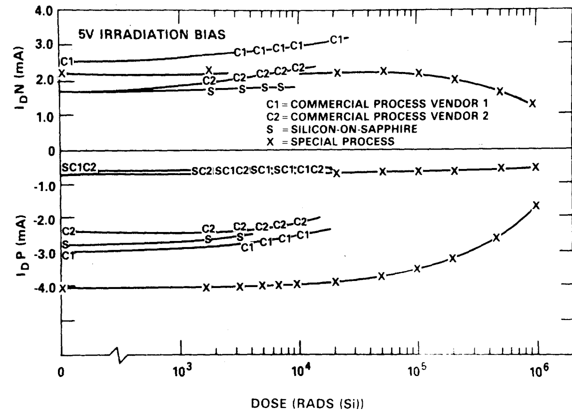

Figure 10. Output drive currents for n- and p-channel transistors versus total dose for 1802s.

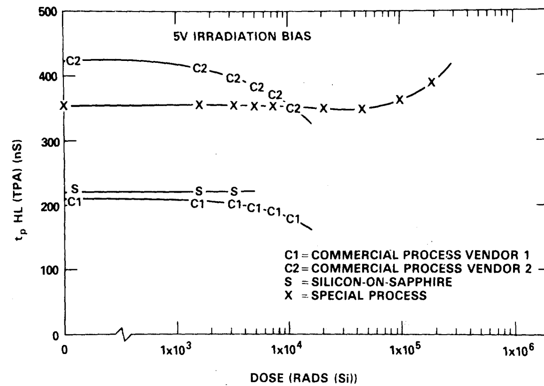

Figure 11. Example of propagation delay variations versus total dose for 1802 devices.

Five other timing measurements were made routinely during the 1802 testing which were defined in Figure 6. Results very similar to those shown in Figure 11 were obtained for these other measurements; thus, the data was not included here.

Analysis

When the SOS and production parts failed, they failed in a catastrophic manner. That is, when they began to fail the low voltage functional test they also began to fail the high voltage functional test, the noise margin tests and many of the current measurements. This catastrophic failure occurs because the n-channel transistors cannot turn completely off after their threshold voltage has become negative. This problem is, of course, independent of the supply voltage or the speed of operation.

On the other hand, the radiation-hard units experienced a very soft failure. As the dose increased, the parts would first fail the 2.8 volt functional test, then the 3.5 volt functional test and next the 5 volt functional test. Note that these devices had not failed the 15 volt functional test even at the 1 Mrad(Si) level. In the same way, problems with timing for the hardened parts were soft also. For example, after the 1 Mrad(Si) dose point the units would not operate with a 1 MHz clock and a 5 volt supply; however, the devices still would perform functionally fairly well at 5 volts if the speed was decreased to a few hundred kHz.

This soft failure behavior of the radiation-hardened 1802s is caused by the continuing negative shifts of the p-channel transistor threshold voltages as the

total dose increases. Apparently there is no problem with any of the n-channels becoming depletion mode and producing a hard failure. This is consistent with the data in Figure 8. However, some of the p-channel transistors must shift more than the data in Figure 8 indicates. For example, in order to explain the soft failure, some of the p-channel thresholds must have shifted to approximately -5 volts at the 5 x 10^5 rad(Si) level. This threshold shift would either keep gates from switching entirely at 5 volts or at least slow their switching speed to the point where the 5 volt functional test indicates failure. That these greater shifts in threshold voltage have occurred is reasonable, since it is observed that gates biased with a low input during irradiation exhibit greater shifts in p-channel threshold voltage than gates which are clocked during irradiation.[3]

Conclusions

Total dose radiation testing on current production line 1802s has indicated that failure of these parts occurs between 8 and 15 krads(Si) for a 5 volt irradiation bias and a 5 volt functional test. The failure level is reduced 20 to 30% if the irradiation bias is increased to 10 volts. Failure level for these parts is related simply to the dose where the n-channel transistors become depletion mode and gates cease to switch effectively.

The failure level of the developmental SOS part tested in this experiment compared favorably with the failure levels for the commercial bulk devices. This suggests that the future 1802 SOS product also may be as hard as the current bulk product.

The results for the 1802s specially processed to increase radiation hardness were very impressive. This is especially encouraging since there has been a fundamental question concerning whether it was possible to harden any Si-gate process to the Mrad(Si) level with present knowledge. The improvement in failure level for these parts was acheived by simple modifications of the standard production line process. N-channel threshold shifts were quite acceptable even at the 1 Mrad(Si) level. Failure in these devices appeared to be entirely determined by the shift in p-channel thresholds which must have been approximately 4 volts at 5 x 10^5 rads (Si) for the -5 volt bias condition. For these devices, since the failure is quite soft, increased operating voltage and/or reduced speed will extend the failure level to some extent. In addition, reduction of p-channel threshold shifts in future lots to values readily acheived using other radiation-hard processes should provide 1802s capable of operation at 1 Mrads (Si) and beyond.

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References

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